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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/516,800	03/01/2000	Thomas J. Kolze	12-1038	2502

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	

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14

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/516,800	KOLZE ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE and amendments filed on 3/26/04 in which claims 1-30 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burch et al U.S. Patent No 5,680,422 in view of Nah et al U.S. Patent No 6,031,886 and in further view of Gaudet U.S. Patent No 6,285,726 B1.

As per claims 1 and 16, Burch et al discloses a communication system, apparatus for transporting a plurality of sampled signals asynchronously from a first location to a second location comprising in combination (see figs. 1-7: a source of one or more data signals (see fig.6 element 51) and one or more clock signals (see fig.6 element 54) at said first location (see figs. 2, 6 elements 26, 50); a reference clock generating (see fig.6 element 136 and col.6, lines 54-60) signal at said first location (see figs. 2, 6 elements 26, 50); a phase comparator is functionally equivalent to the claimed (phase difference estimator) (see fig.6 element 137 and col.6, lines 53-67 and col.7, lines 11-20) for generating a phase signal representing at least an estimate of the difference in phase between one of said clock signals and one of said reference signals; a communication

channel transmitting (see fig.2 element 28 and col.1, line 62) said one or more data signals, said one or more clock signals and said phase signal asynchronously (see abstract) to said second location.

However Burch et al does not teach a plurality of reference clocks generating a plurality of reference signals and estimating a phase difference between said clock signals and said plurality of said reference signals.

Nah et al teaches a mulit-clock generator for generating a plurality of clock signals and a phase comparator is functionally equivalent to the claimed (a plurality of reference clocks generating a plurality of reference signals and estimating a phase difference between said clock signals and said plurality of said reference signals) (see fig.2 elements 1 and 401, 402, respectively).

It would have been obvious to one of ordinary skill in the art to implement the teaching of Nah into Burch as to detect all the transition of external input data occurring between one period of the source clock SC as taught by Nah (see col.6, lines 12-14).

However Burch and Nah in combination do not teach a resampler filter located at said second location; a selector responsive to said phase signal for conditioning the resample filter in response to said phase signal, said conditioned resample filter being responsive to said one ore more data signals for generating one ore more resampled data signals at the second location.

Gauchet teaches an interpolator is functionally equivalent to the claimed (resampler filter) (see fig.5 element 106 and col.6, lines 15, 30) located at said second location; a selector (see fig.5 element 140 or 136 and col.8, lines 23-67 and col.9, lines 5-15) responsive to said phase signal for conditioning the resample filter in response to said

phase signal, said conditioned resample filter being responsive to said one ore more data signals for generating one ore more resampled data signals at the second location.

It would have been obvious to one of ordinary skill in the art to incorporate the resample filter and the selector of Gauchet in to Burch and Nah as to adjust the clock signal by selecting a different phase of N available phases that are provided by a clock generation using an N:1 phase multiplexer and a secondary mux that provides further phase resolution using the interpolator as taught by Gauchet (see col.5, lines 60-64).

As per claims 2-5, the apparatus of Burch et al does include a memory or buffer (see fig.6 element 55). Furthermore implement such memory in a selector would have been obvious to one skilled in the art so that N available different phases which are stored in the memory could be appropriately selected to adjust the clock signal.

As per claim 6, the apparatus of Burch et al does include a second source or more clock signals located at the second location (see fig.7 element 150). However implementing such apparatus to clock one or more data signals from said resample filter would have obvious to one skilled in the art so that phase adjustment of data signals could accurately be determined during the operation.

As per claim 7, the apparatus of Burch et al does include a plurality of multiplexed data signals and a demultiplexer (see figs 1-7).

As per claim 8, the apparatus of Burch et al does include extracting frame synch signal signals (see fig.6 element 53).

As per claim 9, the apparatus of Burch would include a first divided clock signal having a first frequency and a second divided clock signal having a second frequency so

that the phase estimator could indicate whether a predefined edge of the write clock precede or follow a corresponding predefined edge of the reference clock.

As per claim 10, the apparatus of Burch et al does include a data insertion module (see fig.6 element 55 or 52).

As per claim 11, the apparatus of Burch et al does include frame synch signals (see fig.6 element 53).

As per claim 12, the apparatus of Burch et al does include a phase difference estimator (see fig.6 element 137).

As per claim 13, the apparatus of Burch would include a first divided clock signal having a first frequency and a second divided clock signal having a second frequency so that the phase estimator could indicate whether a predefined edge of the write clock precede or follow a corresponding predefined edge of the reference clock.

As per claim 14, the apparatus of Burch et al would include a packetizing module to transmit said data signals as to enhance the system capability and further facilitate the synchronization the data signals at different phases during the operation.

As per claim 15, the apparatus of Burch et al does include a plurality of multiplexed data signals (see figs. 1-7).

As per claims 17-19, the apparatus of Burch et al does include a memory or buffer or storage (see fig.6 element 55). Furthermore implement such memory in a conditioning would have been obvious to one skilled in the art so that N available different phases which are stored in the memory could be appropriately selected to adjust the clock signal.

As per claim 20, the apparatus of Burch et al does include a storing element (see fig.6 element 55).

As per claim 21, the apparatus of Burch et al does include an unsynchronized clocking with said data signal at the first location (fig.6 element 51).

As per claims 22 and 30, the apparatus of Burch et al does include a plurality of multiplexed data signals and a demultiplexer (see figs 1-7).

As per claims 23, 26 and 27, the apparatus of Burch et al does include frame synch from said multiplexer (see fig.6 element 53).

As per claims 24 and 28, the apparatus of Burch would include a first divided clock signal having a first frequency and a second divided clock signal having a second frequency so that the phase estimator could indicate whether a predefined edge of the write clock precede or follow a corresponding predefined edge of the reference clock.

As per claim 25, the apparatus of Burch et al does include inserting said phase signal into said plurality of channels (see figs. 1-6).

As per claim 29, the apparatus of Burch et al would include transmitting said data signals, said clock signal and said phase signal in packets to said second location as to enhance the system capability and further facilitate the synchronization the data signals at different phases during the operation.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is (703) 308-

9573. The examiner can normally be reached on Monday-Thursday from 8:00 AM - 5:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour, can be reached on (703) 306-3034. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3800.

Emmanuel Bayard

Primary Examiner

6/5/04

EMMANUEL BAYARD
PRIMARY EXAMINER